具有NiO异质结和叉指栅柱调制的抗单粒子Ga_2O_3 MOSFET

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摘 要：本文提出了一种具备抗单粒子烧毁(Single-Event Burnout，SEB)能力的复合叉指栅柱结构氧化镓金属氧化物半导体场效应晶体管(Comb-Shaped Gate Metal-Oxide-Semiconductor Field-Effect Transistor，CSG-MOSFET)。该器件在N型Ga_2O_3沟道层上方引入P型NiO层，并通过叉指栅柱将其与延伸栅场板实现电气连接。基于P-NiO/N-Ga_2O_3异质结的电荷补偿效应，该结构显著优化了沟道内的电场分布。同时，叉指栅柱作为关键的电场调制单元，与延伸场板协同作用，不仅有效抑制了传统器件(Conventional-MOSFET，C-MOSFET)中栅极场板边缘的电场拥挤效应，更将易诱发单粒子雪崩击穿的峰值电场区域从脆弱的栅极边缘主动转移至最外侧栅柱边缘。TCAD仿真结果表明，在重离子辐照下，所提出的CSG-MOSFET将其SEB阈值电压(V_{SEB})从传统器件的240 V大幅提升至2280 V，充分证实了该复合结构在提升Ga_2O_3功率器件抗辐射性能方面的优势。

关键词：Ga_2O_3 MOSFET；抗辐照加固；叉指栅柱

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1 引言

凭借超宽禁带(约4.8 eV)与超高临界击穿电场(约8 MV/cm)等卓越的材料特性，氧化镓(Ga_2O_3)金属氧化物半导体场效应晶体管(MOSFET)已成为航空航天与卫星平台等空间功率电子应用中备受瞩目的核心器件[1]。然而，复杂的空间辐射环境中充斥着高能重离子、质子及宇宙射线，极易在器件内部诱发单粒子效应(Single-Event Effect, SEE)。这不仅会导致器件电学性能急剧退化，甚至可能引发不可逆的单粒子烧毁(Single-Event Burnout, SEB)，严重制约了Ga_2O_3功率器件在轨运行的可靠性[2,3]。因此，深入揭示Ga_2O_3 MOSFET的SEB物理机理并探索行之有效的加固设计方法，已成为推动其空间应用进程的关键科学问题。

目前，针对Ga_2O_3器件抗单粒子辐照的研究尚处于起步阶段，相关物理机制的仿真揭示与实验验证仍显不足[4]。更严重的是，Ga_2O_3材料的本征属性进一步加剧了抗辐照加固设计的挑战。一方面，Ga_2O_3极低的热导率导致重离子穿透产生的瞬态焦耳热难以有效耗散，极易在局部形成热点，使得横向器件在辐照下更容易发生电流崩塌与热力学烧毁[5,6]；另一方面，Ga_2O_3难以实现高效、稳定的P型掺杂，这直接限制了传统结终端扩展(Junction Termination Extension, JTE)、结隔离等成熟抗辐照技术的移植与应用，导致电离产生的过剩载流子极易在场板边缘等敏感区域大量聚集[7,8]。现有的SEB加固方案多局限于传统的场板结构优化或介质层工程[9–11]，尚未形成系统体系。尽管引入P型氧化物(如NiO)形成异质结已被证明是克服Ga_2O_3缺乏P型掺杂的有效途径，但将其应用于抗辐照加固领域的研究仍鲜有报道。因此，亟需探索新型结构以突破横向Ga_2O_3 MOSFET的抗单粒子性能瓶颈。

基于上述现状，本文创新性地提出了一种融合异质结与叉指栅柱复合结构的抗单粒子器件(Comb-Shaped Gate Metal-Oxide-Semiconductor Field-Effect Transistor, CSG-MOSFET)，并借助TCAD仿真平台对其基础电学特性与抗SEB机理进行了系统研究。结果表明，相较于传统器件(Conventional-MOSFET, C-MOSFET)，所提出的CSG-MOSFET不仅在击穿电压(Breakdown Voltage，*BV*)上具有优势，更实现了SEB阈值电压(SEB Threshold Voltage，V_{SEB})的大幅跃升。本研究为Ga_2O_3功率器件在强辐射环境下的高可靠性结构设计提供了全新的理论依据与技术途径。

2 器件结构与机理

图1(a)展示了C-MOSFET的横截面结构示意图，自下而上依次包括：Ga_2O_3衬底、N型Ga_2O_3沟道层、N^+氧化镓重掺杂源漏区、SiO_2介电层,其

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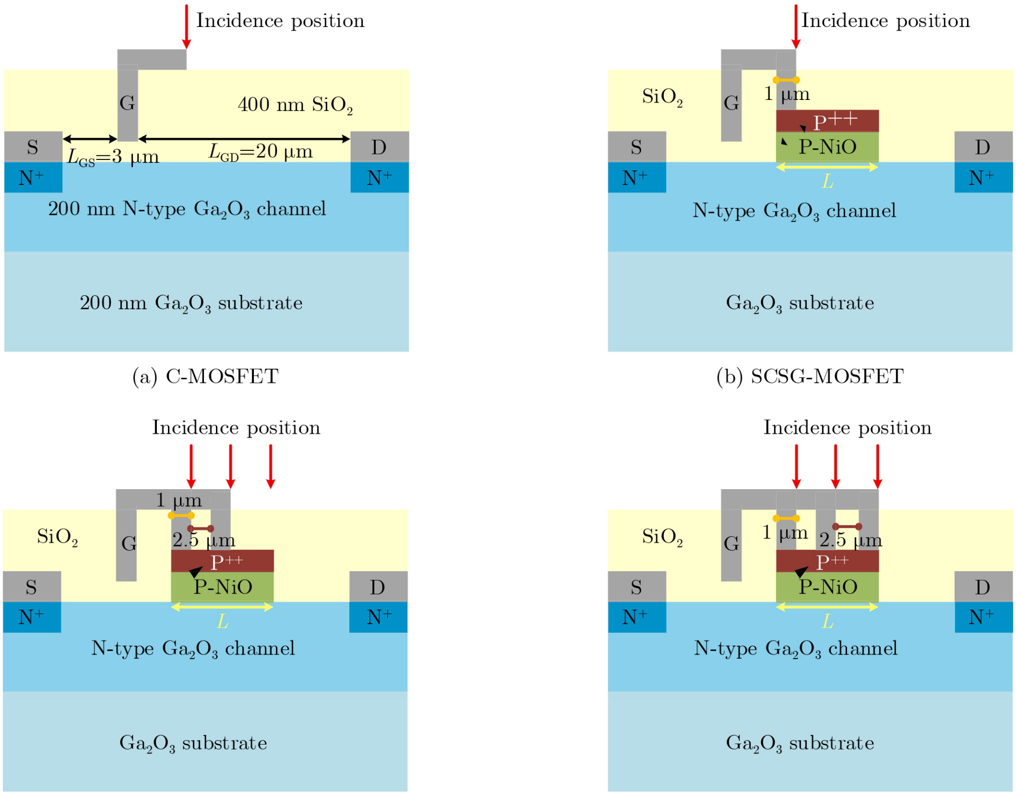


(a) C-MOSFET (b) SCSG-MOSFET (c) DCSG-MOSFET (d) TCSG-MOSFET

图 1 器件截面图，(a) C-MOSFET、(b) SCSG-MOSFET、(c) DCSG-MOSFET和 (d)TCSG-MOSFET

中N^+氧化镓重掺杂源漏区分别和源极、漏极金属形成欧姆接触。图1(b–d)展示了所提出的具有单叉指栅柱(Single Comb-Shaped Gate MOSFET, SCSG-MOSFET)、双叉指栅柱(Double Comb-Shaped Gate, DCSG-MOSFET)与三叉指栅柱(Triple Comb-Shaped Gate, TCSG-MOSFET)复合结构的三种器件。在N型Ga_2O_3沟道层上方依次设置低掺杂P型NiO层与高掺杂P型NiO层，其中高掺杂层用于与叉指栅柱形成良好欧姆接触以确保可靠电气连接，同时基于P-NiO/N-Ga_2O_3异质结的电荷补偿效应优化沟道内的电场分布；随后通过增加栅柱数量(各栅柱宽1 μm、间距为2.5 μm)并将栅极场板延伸至新增栅柱边缘，有效缓解栅极场板边缘的电场集中效应，具体参数见表1。

本文采用二维TCAD工具研究Ga_2O_3 MOSFET的电学特性和单粒子烧毁特性。为准确描述器件的输运、复合及击穿行为，仿真中引入fldmob迁移率模型、Shockley Read Hall复合模型、Auger复合模型和碰撞电离模型[12,13]。SEB仿真采用HeavyIon模型，重离子辐照条件设定为线性能量转移(Linear Energy Transfer, LET)为85.7 $MeV\cdot cm^2/mg$[14]，该值是美国国家航空航天局(National Aeronautics and Space Administration, NASA)、欧洲空间局(European Space Agency, ESA)及相关军用标准中常用的单粒子效应评估参考点，便于不同器件和研究结果之间的对比。需要指出的是，LET仅表征单位路径上的总能量沉积，而相同LET下不同原子序数Z的离子仍可能具有不同的径迹结构和径向电荷沉积分布；在TCAD仿真中，这类差异主要通过载流子产生率的空间高斯分布参数体现[15]。因此，本文采用钽(Ta)离子作为入射粒子，其Z=73，可代表高Z重离子条件下较强电荷沉积和显著径迹扰动的辐照响应。为降低变量复杂度，重离子设定为垂直入射并完全贯穿器件结构。

表 1 所有器件的主要参数

器件参数	数值
N型Ga_2O_3沟道掺杂浓度	5×10^{17} cm^{-3}
N^+区掺杂浓度	1×10^{19} cm^{-3}
N^+区厚度	50 nm
P-NiO区厚度	80 nm
P-NiO区长度 (L)	Variable
P-NiO区掺杂浓度(N_A)	Variable
P^{++}区厚度	10 nm
P^{++}区掺杂浓度	1×10^{19} cm^{-3}

3　仿真结果与分析

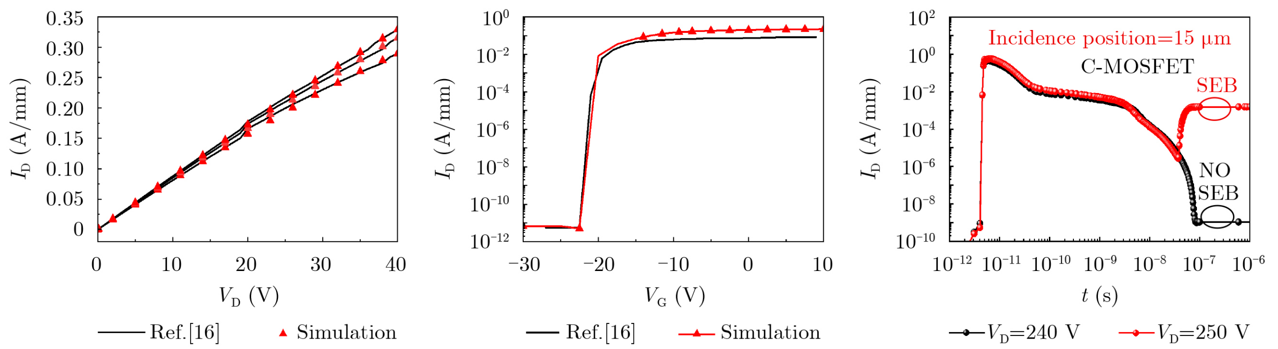
3.1　C-MOSFET的电学及SEB特性

为验证所建TCAD仿真模型及物理参数设置的准确性，本文首先将C-MOSFET的输出特性与文献[16]中的数据进行了对标校准。如图2(a)与图2(b)所示，本文的仿真结果与参考数据拟合度高，充分证明了所采用物理模型的合理性。在偏置条件为V_G=5 V、V_D=25 V时，器件提取的阈值电压(V_{th})为-20 V，漏极电流密度(I_D)达到0.335 A/mm。在完成模型校验后，为深入探究C-MOSFET的SEB行为，本文基于前期研究确定的器件最敏感区域，选取x=15 μm(即栅极场板边缘处)作为入射点，引入LET=85.7 MeV·cm²/mg的重离子进行辐照模拟[16]。图2(c)展示了C-MOSFET在关态(V_{GS}=-25 V)条件下，器件发生SEB前后的漏极瞬态电流响应特性。当V_D为240 V时，重离子撞击诱发的瞬态电流在经历脉冲尖峰后能够逐渐衰减，并最终恢复至初始的低泄漏电流态；然而，当V_D升高至250 V时，漏极电流在撞击后无法恢复，发生持续性激增并稳定在1 mA/mm的失效安全阈值之上，标志着器件内部发生了不可逆的烧毁。由此可判定，C-MOSFET的V_{SEB}为240 V。

图3与图4分别揭示了C-MOSFET在重离子入射后的瞬态电子和空穴演变过程。在t=5×10^{-12} s撞击瞬间，沿入射径迹产生了高密度的电子-空穴对。随后，在漏极偏压驱动下，电子与空穴分别向漏极和源极快速漂移。如图5(a)所示，瞬态电荷的移动引发了显著的电场调制效应，导致电场峰值高度拥挤在栅极正下方及入射径迹周围，极易诱发强烈的雪崩击穿。图5(b–e)的碰撞电离率分布进一步证实了这一过程：撞击初期，碰撞电离局限于径迹附近；但随着载流子在栅极下方的不断积累，局部电场被进一步畸变放大，导致碰撞电离率增大。这种正反馈机制最终引发栅下沟道的寄生导通，使得漏极电流彻底失控并持续超过1 mA/mm的安全阈值，标志器件发生SEB失效。

3.2　SCSG-MOSFET的电学及SEB特性

为克服C-MOSFET抗SEB能力的不足，本文



(a) 根据文献[16]拟合的转移特性曲线　(b) 根据文献[16]拟合的输出特性曲线　(c) C-MOSFET器件发生SEB前后的瞬态漏极电流曲线

图 2 C-MOSFET与文献[16]的拟合

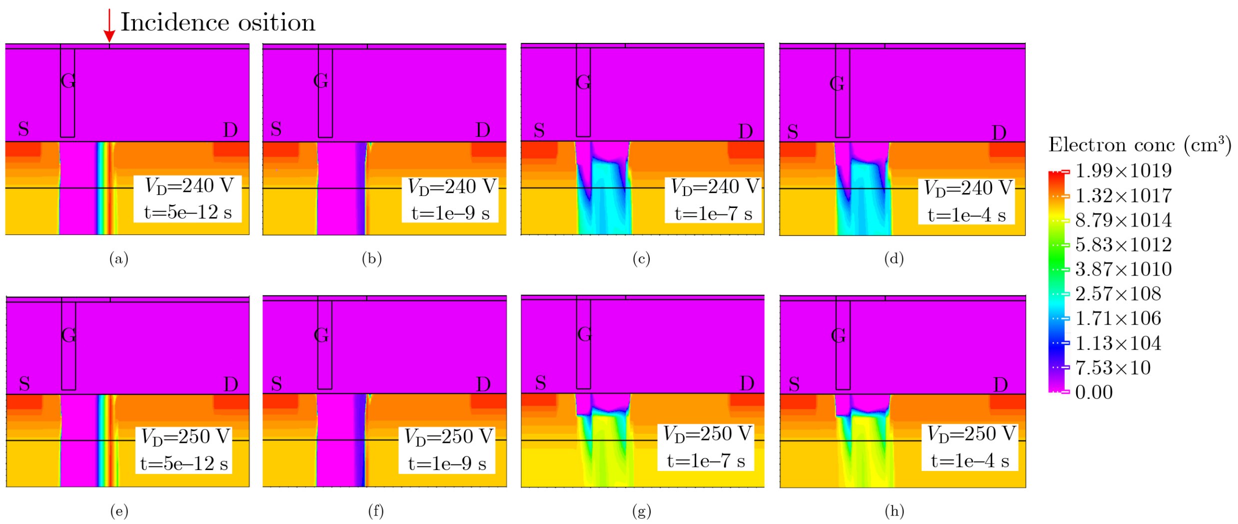


图 3 C-MOSFET发生SEB前后不同时刻下的电子浓度分布图

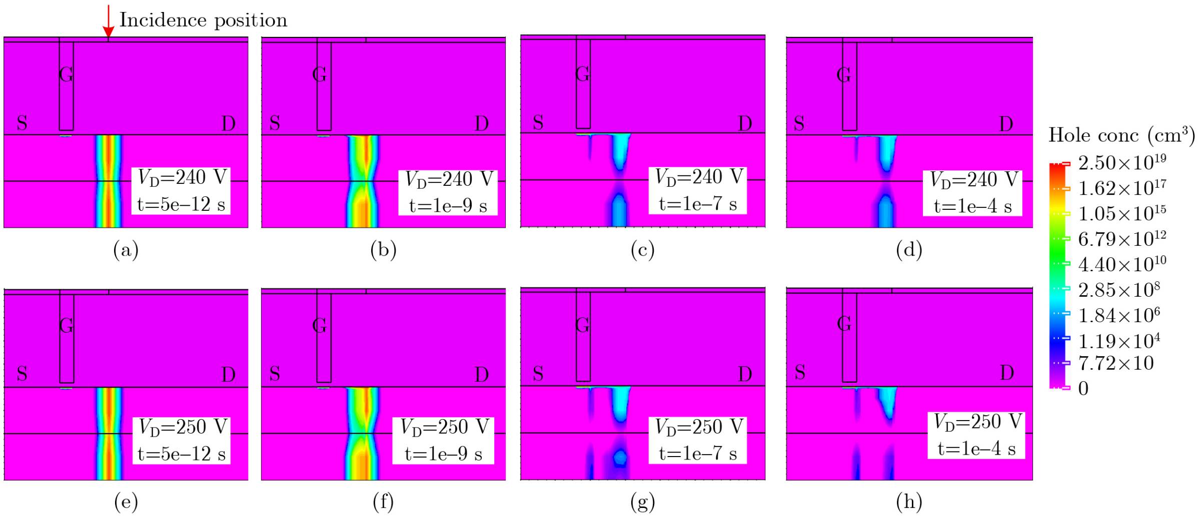
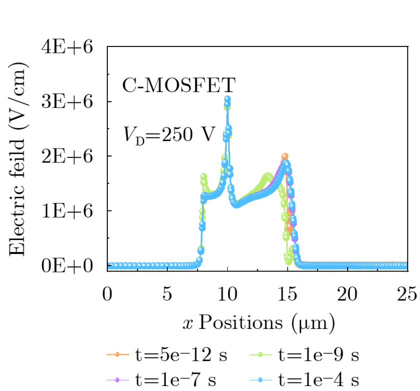
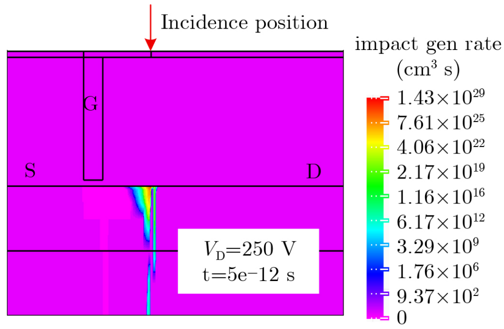


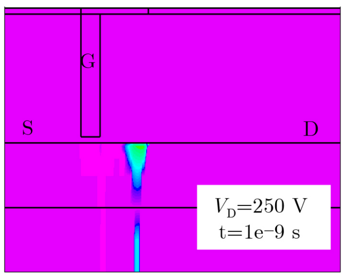
图 4 C-MOSFET发生SEB前后不同时刻下的空穴浓度分布图



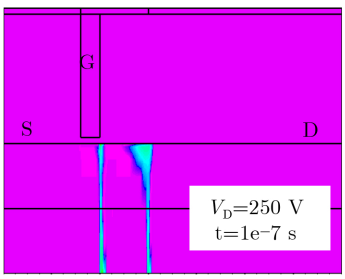
(a) V_D=250 V时不同时刻下的电场分布曲线



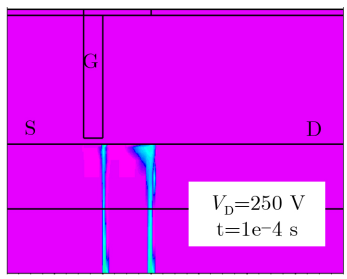
(b) V_D=250 V，t=5e–12 s时的碰撞生成率



(c) V_D=250 V，t=1e–9 s时的碰撞生成率



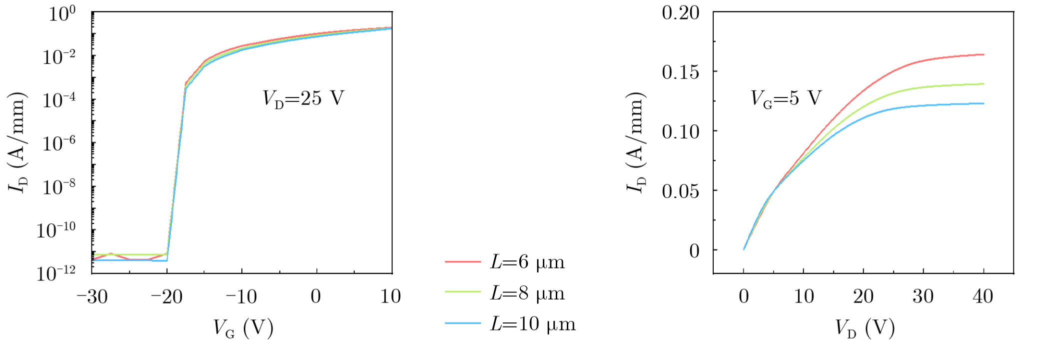
(d) V_D=250 V，t=1e–7 s时的碰撞生成率



(e) V_D=250 V，t=1e–4 s时的碰撞生成率

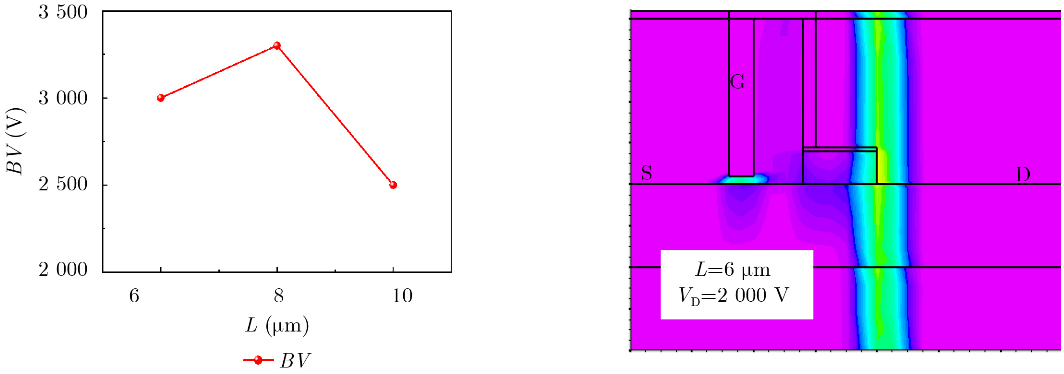
图 5 C-MOSFET在V_D=250 V时不同时刻下的电场分布曲线与碰撞生成率

首先提出了图1(b)所示的SCSG-MOSFET。该结构利用P-NiO/N-Ga_2O_3异质结的电荷补偿效应，有效优化了沟道内的电场分布。为此，本文对比分析了NiO长度(L=6，8，10 μm)对器件特性的影响。此过程中，P-NiO的掺杂浓度N_A设定的初始值为8e17 cm^{-3}，其与沟道掺杂浓度在一个数量级[17]，通过在后续进一步优化P-NiO中的掺杂浓度，从而最终确定其最优值。图6的转移与输出特性表明，随着NiO长度增加，异质结对底层沟道的耗尽作用加剧，导致I_D显著下降。图7进一步展示了SCSG-MOSFET在关态条件下(V_G=-25 V)，V_D=2000 V时不同L值对器件内部电场分布的影响。随着L增大，器件的峰值电场逐渐向漏极一侧移动。在L分别为6 μm、8 μm和10 μm时，对应的击穿电压BV分别为3 000 V、3 300 V和2 500 V，相较于传统C-MOSFET的2000 V分别提高了50%、65%和25%。当L增加至10 μm时，BV出现下降的原因在于峰值电场过度靠近漏极，导致承担高压的有效区域减小，从而削弱了器件的耐压能力。考虑到L=10 μm时正向导通特性的显著退化以及耐压性能的下降，

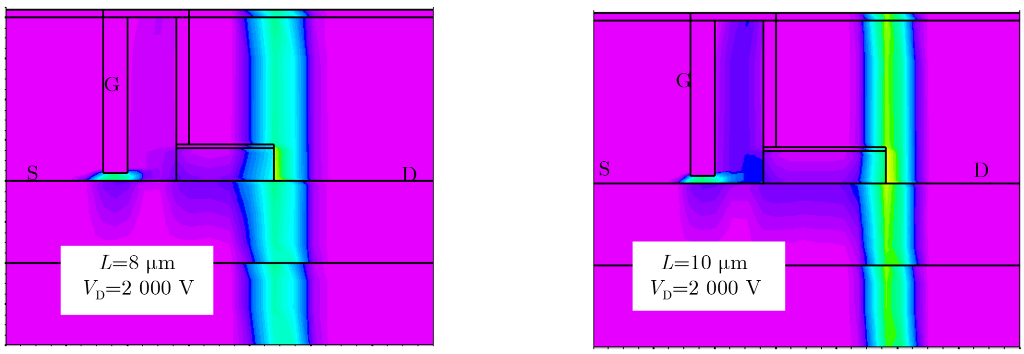


(a) 不同NiO长度L下的转移特性曲线　　(b) 不同NiO长度L下的输出特性曲线

图 6 SCSG-MOSFET中不同L下的导通特性



(a) 不同NiO长度L下的BV值对比　　(b) 关态下L=6 μm，V_D=2 000 V时的电场分布



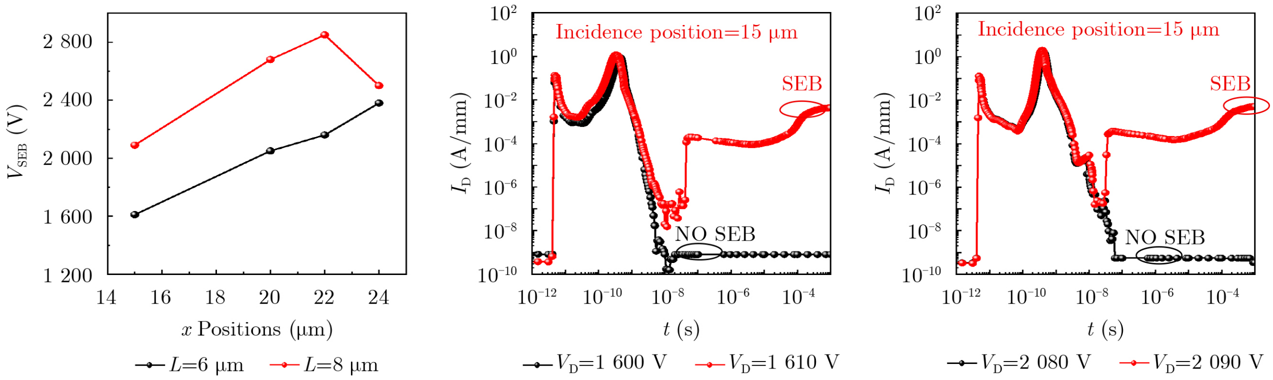
(c) 关态下L=8 μm，V_D=2 000 V时的电场分布　　(d) 关态下L=10 μm，V_D=2 000 V时的电场分布

图 7 不同L值对SCSG-MOSFET的BV及电场分布影响

后续SEB研究仅选取L=6 μm和L=8 μm两种尺寸，以兼顾器件的综合性能。图8(a)评估了不同入射位置下的V_{SEB}，图8(b)与图8(c)分别展示了未发生与发生SEB的瞬态电流曲线。结果显示，两种尺寸器件的辐照最敏感点均位于x=15 μm(即新增栅柱外侧边缘)。最终，采用6 μm NiO的器件V_{SEB}为1 600 V；当NiO增至8 μm时，V_{SEB}进一步提升至2080 V，展现出显著的抗辐照加固效果。

图9与图10展示了SCSG-MOSFET发生SEB前后不同时刻下的载流子浓度分布，可以发现P-NiO层对下方Ga_2O_3沟道形成了显著的耗尽调制。借助新增栅柱对耗尽区的增强控制，器件在瞬态过程中有效拓宽了电流路径。强电场作用下，电子与空穴分别向漏极和栅极快速漂移，使得原本局域化的碰撞电离被分散至整个NiO覆盖区下方，避免了局部雪崩激增。图11进一步揭示了改善电场分布的内在机制：P-NiO与N-Ga_2O_3间的电荷补偿效应。该异质结通过电荷耦合作用，有效缓解了传统C-MOSFET中栅极边缘的电场拥挤，将尖锐的电场峰值重塑为均匀平滑的分布轮廓，从而显著增强了器件的抗SEB鲁棒性。综合衡量BV、V_{SEB}及导通损耗等关键指标，本文选取综合性能最优的8 μm NiO结构开展后续深入研究。

确定最优长度后，本文进一步对L=8 μm的



(a) 不同NiO长度L下的VSEB值对比　(b) L=6 μm时发生SEB前后的瞬态漏极电流曲线　(c) L=8 μm时发生SEB前后的瞬态漏极电流曲线

图 8 SCSG-MOSFET中V_{SEB}值对比与瞬态漏极电流曲线

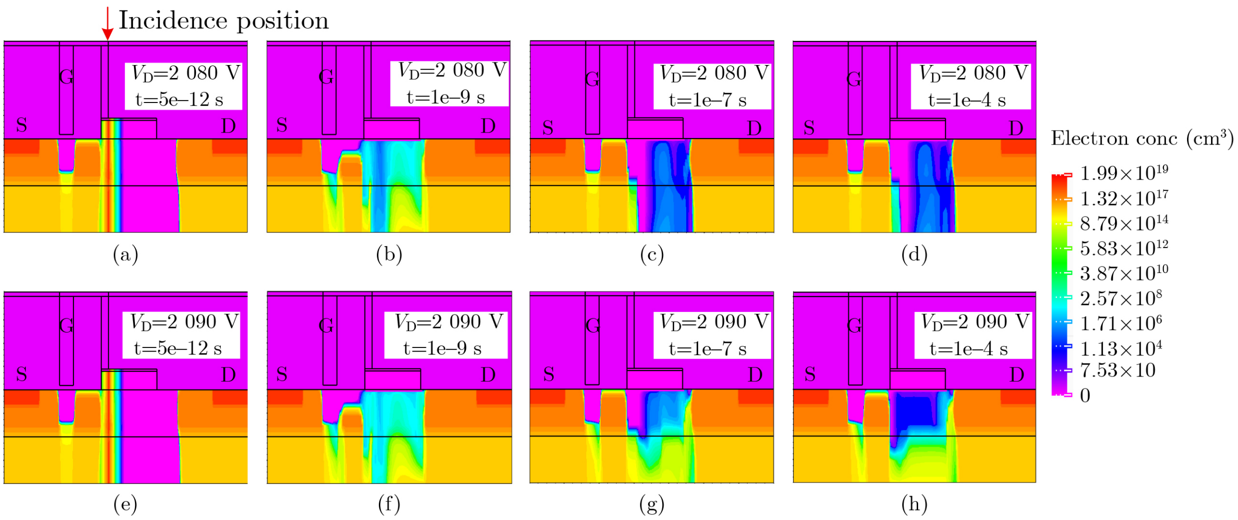


图 9 SCSG-MOSFET发生SEB前后不同时刻下的电子浓度分布图

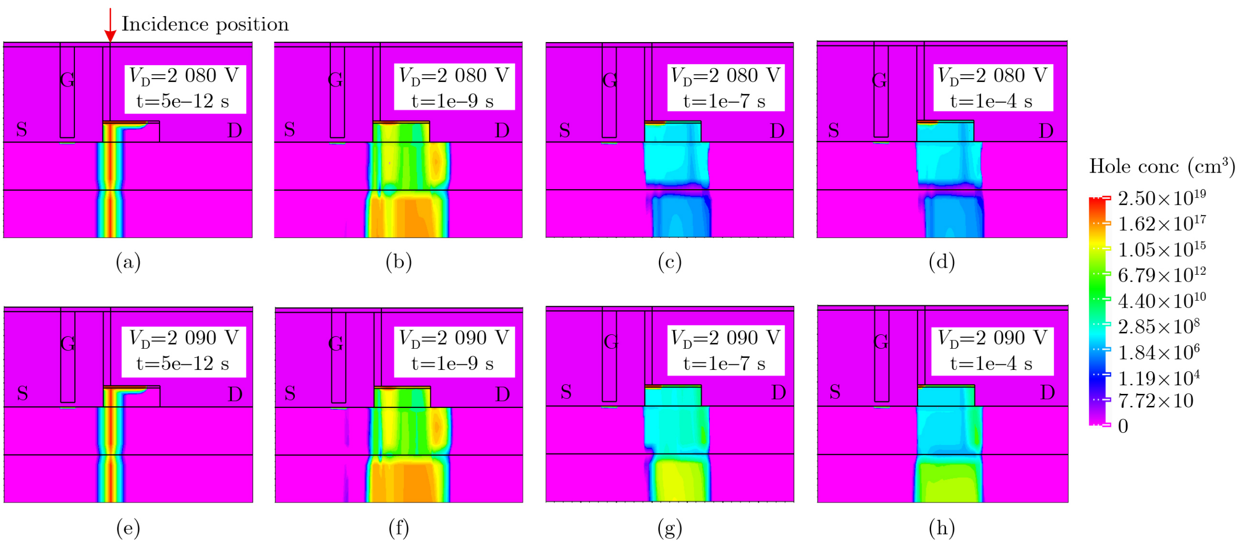
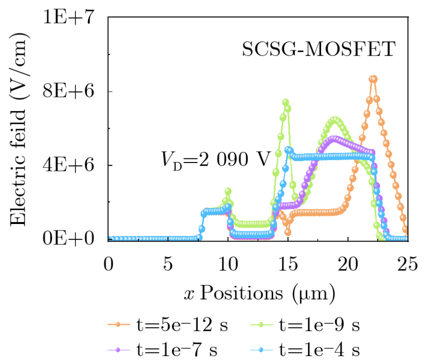
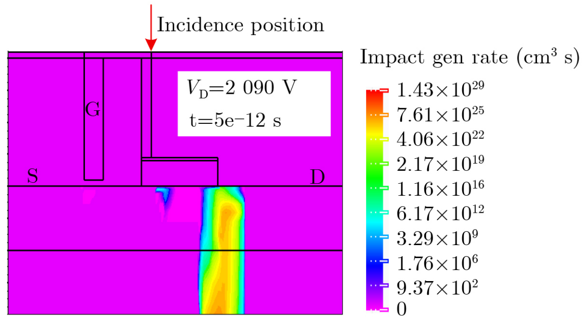


图 10 SCSG-MOSFET发生SEB前后不同时刻下的空穴浓度分布图

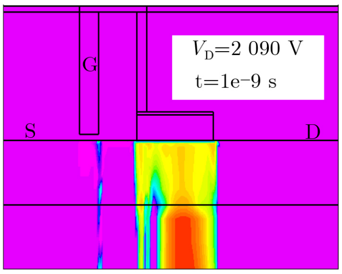
N_A开展优化。由于异质结通过电荷补偿调制电场，N_A的改变将深刻影响耗尽区的宽度与电荷平衡强度。图12与图13分别展示了不同浓度下SCSG-MOSFET的直流特性与抗SEB能力对比。结果显示，随着N_A从8×10^{17} cm^{-3}降低至1×10^{16} cm^{-3}，器件的V_{th}从−16.5 V负向漂移至-20 V，I_D从0.141 A/mm



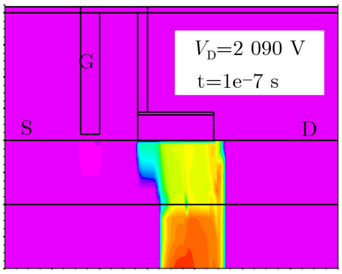
(a) V_D=2090 V时不同时刻下的电场分布曲线



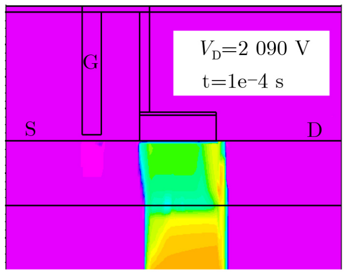
(b) V_D=2 090 V，t=5e−12 s时的碰撞生成率



(c) V_D=2 090 V，t=1e−9 s时的碰撞生成率

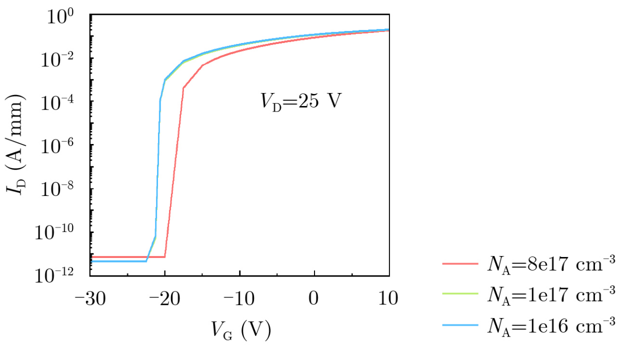


(d) V_D=2 090 V，t=1e−7 s时的碰撞生成率

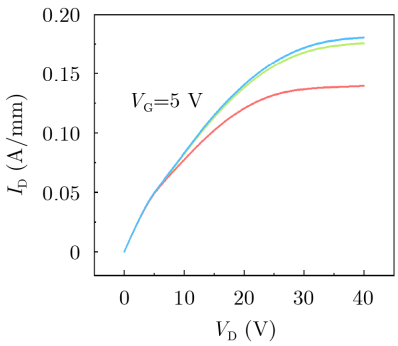


(e) V_D=2 090 V，t=1e−4 s时的碰撞生成率

图 11 SCSG-MOSFET在V_D=2090 V时不同时刻下的电场分布曲线与碰撞生成率



(a) 不同NiO浓度N_A下的转移特性曲线



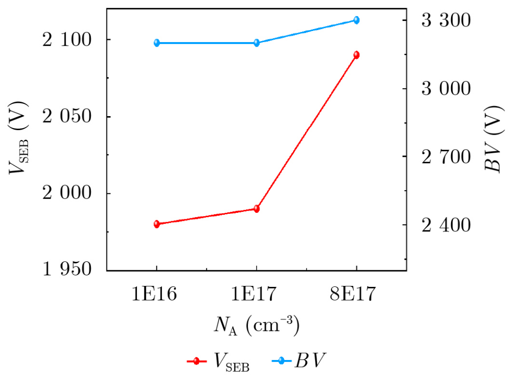
(b) 不同NiO浓度N_A下的输出特性曲线

图 12 SCSG-MOSFET中不同N_A下的导通特性

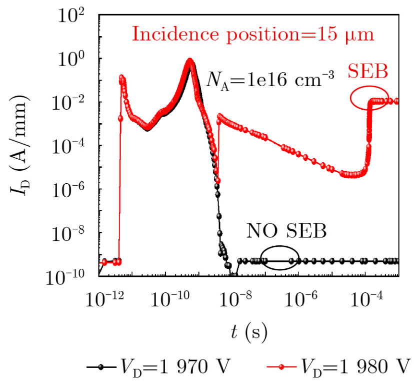
增至0.181 A/mm。同时，器件的BV从3 300 V略降至3 200 V，敏感位置(x=15 μm)处的V_{SEB}降至1970 V。这种性能的折中可归因于：较低的P-NiO浓度减弱了对下方沟道的耗尽作用，使得导电路径变宽，从而改善了输出电流并导致V_{th}负移；但同时，由于电荷补偿效应的削弱，器件内部电场分布的均匀性有所下降，导致耐压与抗辐照性能出现小幅折损。基于导通与阻断/抗辐照性能的综合权衡，本文最终选取N_A为1×10^{16} cm^{-3}、L=8 μm的参数，并以此开展后续并以此开展后续DCSG-MOSFET与TCSG-MOSFET两种结构的对比研究。

3.3 DCSG-MOSFET与TCSG-MOSFET的电学及SEB特性

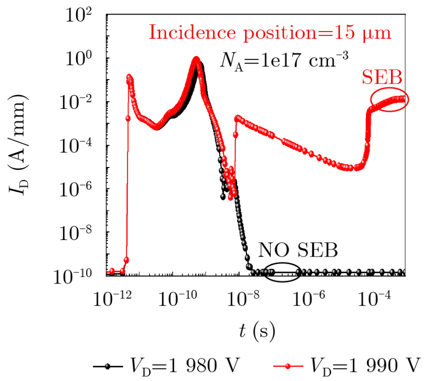
为进一步缓解C-MOSFET栅极场板边缘的电场集中效应，本文对叉指栅极柱的数量进行了优化，设计了如图1(c)的DCSG-MOSFET与图1(d)的TCSG-MOSFET结构。图14与图15的电学特性及瞬态SEB响应表明，栅极柱的引入在维持器件原有V_{th}与输出电流不受影响的前提下，显著改变了内部的峰值电场位置。同时，多级栅柱的引入促使电场峰值从主栅极场板边缘向右侧逐级转移，有效避免了局域强电场集中，如图16所示。仿真结果显示，DCSG-MOSFET的电场峰值与辐照敏感点平移至第二栅极柱右侧边缘(x=18.5 μm)，其对应的BV与V_{SEB}分别达到3 500 V 和2 280 V。然而，对于TCSG-MOSFET，其峰值电场虽移至最右侧NiO边缘(x=22 μm)，但由于该位置过于靠近漏极，导致缓冲高压的有效漂移区长度大幅缩减，反



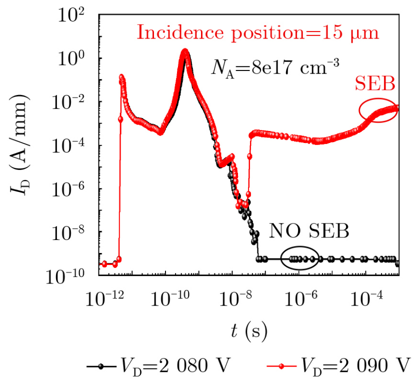
(a) 不同NiO浓度N_A下的V_{SEB}与BV值对比



(b) N_A=1e16 cm^{-3}时发生SEB前后的瞬态漏极电流曲线

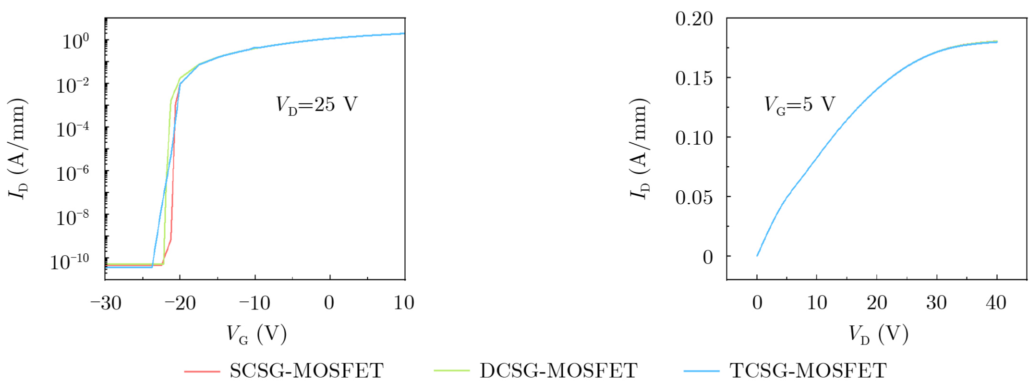


(c) N_A=1e17 cm^{-3}时发生SEB前后的瞬态漏极电流曲线

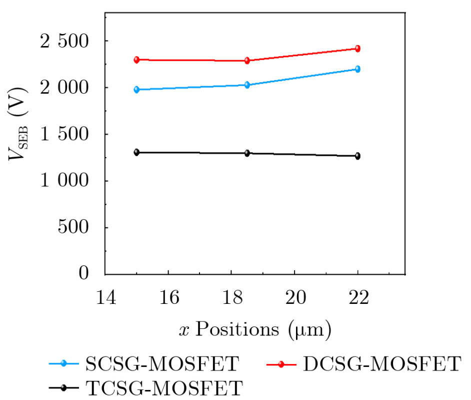


(d) N_A=8e17 cm^{-3}时发生SEB前后的瞬态漏极电流曲线

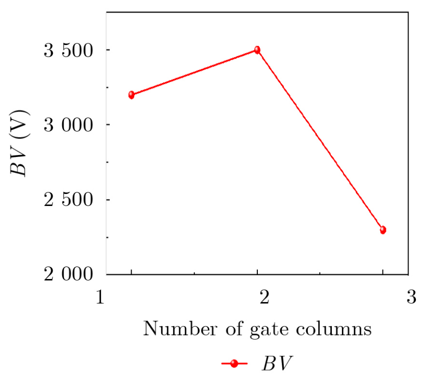
图 13 SCSG-MOSFET中V_{SEB}值对比与瞬态漏极电流曲线



(a) 不同叉指栅柱个数下的转移特性曲线 (b) 不同叉指栅柱个数下的输出特性曲线



(c) 不同叉指栅柱个数下的V_{SEB}值对比

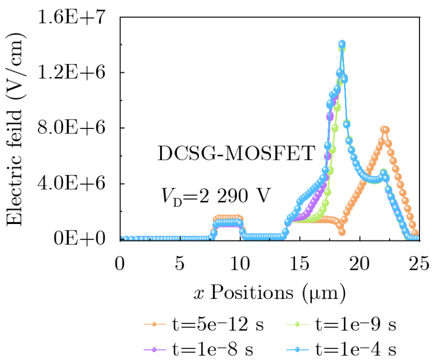


(d) 不同叉指栅柱个数下的BV值对比

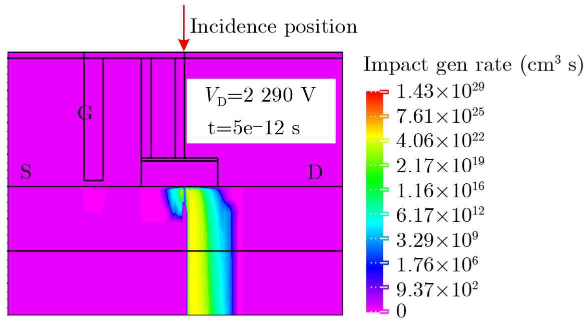
图 14 不同叉指栅柱个数下的基本电学特性与V_{SEB}值对比

而引起耐压与抗辐照性能的退化。因此，DCSG-MOSFET实现了电场分布与性能的最优折中。

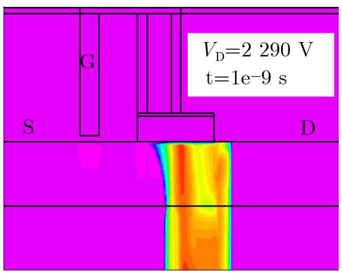
表2汇总了所有器件的核心电学与抗辐照特性参数。定量分析表明，相较于传统的C-MOSFET，本文最终确立的DCSG-MOSFET展现出卓越的综合性能优势。一方面，其BV与V_{SEB}分别实现了



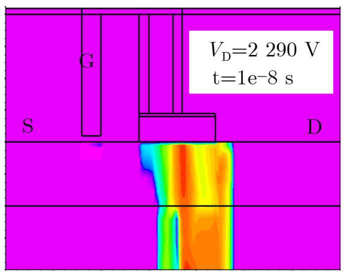
(a) V_D=2 290 V时不同时刻下的电场分布曲线



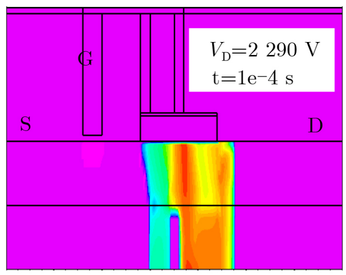
(b) V_D=2 290 V，t=5e−12 s时的碰撞生成率



(c) V_D=2 290 V，t=1e−9 s时的碰撞生成率

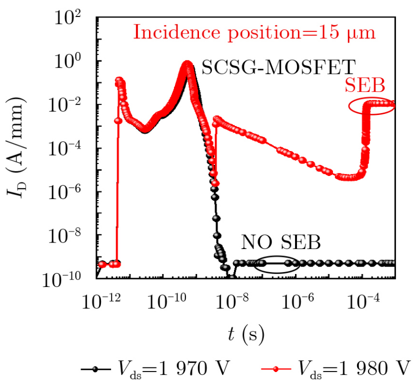


(d) V_D=2 290 V，t=1e−8 s时的碰撞生成率

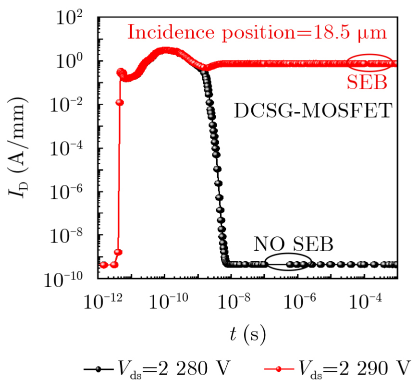


(e) V_D=2 290 V，t=1e−4 s时的碰撞生成率

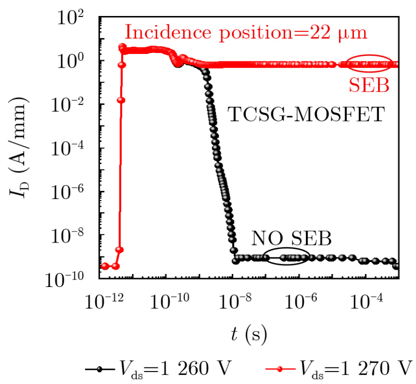
图 16 DCSG-MOSFET在V_D=2 290 V时不同时刻下的电场分布曲线与碰撞生成率



(a) SCSG发生SEB前后的瞬态漏极电流曲线



(b) DCSG发生SEB前后的瞬态漏极电流曲线



(c) TCSG发生SEB前后的瞬态漏极电流曲线

图 15 不同叉指栅柱个数下发生SEB前后的瞬态漏极电流曲线

表 2　所有器件的主要电学特性参数(L=8 μm，N_A=1e16 cm^{-3})

器件特性	C-MOSFET	SCSG-MOSFET	DCSG-MOSFET	TCSG-MOSFET
V_{th}(V)	–20	–20	–20	–20
$R_{on,sp}$(mΩ/cm^2)	39.6	31.4	31.4	31.4
BV(V)	2000	3200	3500	2300
V_{SEB}(V)	240	1970	2280	1260
$BFOM(BV^2/R_{on,sp})$	0.1 GW/cm^2	0.33 GW/cm^2	0.39 GW/cm^2	0.17 GW/cm^2
$BFOM(V_{SEB}^2/R_{on,sp})$	0.001 GW/cm^2	0.12 GW/cm^2	0.17 GW/cm^2	0.05 GW/cm^2

75%与高达850%的显著跃升。另一方面，基于耐压与导通特性评估的综合优值指数(Baliga's Figure of Merit, *BFOM*)计算结果显示，DCSG-MOSFET的*BFOM*值较传统结构也获得了极大的提升。所提出的多级叉指栅异质结架构在维持优异正向导通特性的前提下，实现了器件高压阻断能力与抗单粒子辐射能力的全面优化。

图17展示了所提出的DCSG-MOSFET的制备工艺流程。首先，在半绝缘Ga_2O_3衬底上外延生长N型Ga_2O_3沟道层。随后，通过选择性离子注入结合快速热退火(Rapid Thermal Annealing, RTA)工艺激活杂质，形成低欧姆接触的高掺杂N^+源漏区域。紧接着，在沟道层上方依次沉积轻掺杂(P^-)与重掺杂(P^+)的双层NiO结构，以构建核心的异质结体系。其后，在P-NiO表面覆盖沉积SiO_2作为层间介电层。最后，通过光刻与刻蚀工艺精准打开源极、漏极以及多级叉指栅极的接触窗口，并依次完成金属电极的沉积与表面钝化层的生长，最终实现完整器件的制备。

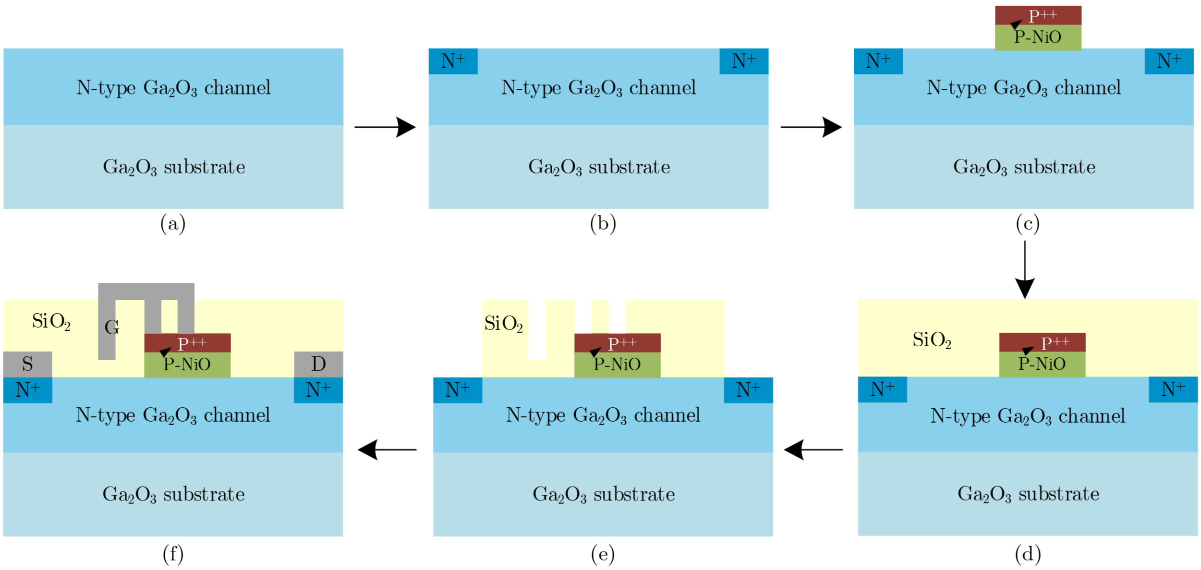


图 17 DCSG-MOSFET的简化制造流程示意图

4 结论

本文提出了一种面向强辐射环境的新型加固多级叉指栅异质结器件DCSG-MOSFET。P-NiO/N-Ga_2O_3异质结凭借卓越的二维电荷补偿效应，从根本上重塑并平滑了沟道层内的电场分布；同时，创新引入的叉指栅柱与延伸场板协同耦合，形成了高效的多级电场调制单元。这种多级电场重构设计消除了诱发早期雪崩击穿的局部热点，极大提升了器件耐压。在LET为85.7 MeV·cm^2/mg 的重离子辐照下，DCSG-MOSFET的V_{SEB}从C-MOSFET的240 V大幅提升至2280 V，提升幅度近850%。本研究不仅揭示了异质结抗辐照设计的内在物理规律，更为超宽禁带Ga_2O_3功率器件迈向航空航天等极端辐射环境应用提供了必要的理论基础与设计准则。

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Radiation-Hardened Ga_2O_3 MOSFET Design Featuring NiO Heterojunction and Comb-Shaped Gate Modulation

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Abstract:

Objective　Gallium Oxide Metal-Oxide-Semiconductor Field-Effect Transistor (Ga_2O_3 MOSFET) is considered a promising power device for high-voltage applications, particularly in space power systems such as aerospace and satellite platforms, owing to its ultra-wide bandgap and high critical breakdown field. However, the Conventional Ga_2O_3 MOSFET (C-MOSFET) exhibits significant drawbacks when operating in space radiation environments. Under off-state conditions, the electric field distribution within the channel region is highly concentrated, particularly at the gate edge, where localized strong electric fields form. When a high-energy heavy ion strikes the device, a large number of electron-hole pairs are generated along the ion track. Under the influence of the strong electric field, these carriers undergo multiplication effects, causing the drain current to surge dramatically and fail to recover, ultimately leading to irreversible Single-Event Burnout (SEB) even at relatively low drain biases. This phenomenon represents one of the primary failure modes for power devices in space applications, severely limiting the reliable deployment of Ga_2O_3 MOSFETs in harsh radiation environments. Furthermore, the difficulty in achieving reliable and efficient P-type doping in Ga_2O_3 inherently limits the application of conventional radiation-hardening techniques such as junction termination extensions and junction isolation in Ga_2O_3 devices. The difficulty in achieving reliable and efficient P-type doping in Ga_2O_3 makes ionized charges more prone to accumulation in sensitive regions, further exacerbating the device's susceptibility to Single-Event Effects (SEE). Meanwhile, the extremely low thermal conductivity of Ga_2O_3 causes Joule heat generated by transient currents to accumulate locally without effective dissipation. Within an extremely short time after heavy-ion incidence, heat concentrates in a microscopic region, forming localized hot spots that significantly increase the risk of thermal-induced burnout. To address these issues, existing hardening approaches such as field plates and dielectric layer optimization provide certain improvements in device robustness, yet research on the application of heterojunction structures for radiation hardening in Ga_2O_3 MOSFETs remains relatively limited, and systematic hardening solutions have yet to be established. While field plates can alleviate the peak electric field at the gate edge, their capability to dissipate transient carriers generated by heavy-ion incidence is limited. Dielectric layer optimization primarily improves the reliability of the gate dielectric but offers weak modulation of the internal electric field within the channel. To address these issues, this paper proposes a radiation-hardened Ga_2O_3 MOSFET featuring a NiO heterojunction and Comb-Shaped Gate (CSG) column structure, which optimizes the electric field distribution within the channel region, alleviates the electric field crowding effect at the conventional gate edge, and significantly enhances the device's SEB robustness, providing an effective solution for Ga_2O_3 power devices in harsh radiation environments.

Methods TCAD simulations are employed to evaluate the electrical characteristics and SEB performance of the proposed CSG-MOSFET, in comparison with the C-MOSFET. A range of physical models is incorporated in the simulations, including high-field mobility saturation, Shockley-Read-Hall and Auger recombination, impact ionization, and heavy-ion incidence. Based on the charge compensation mechanism in the space charge region of a PN junction, the proposed heterojunction structure leverages the depletion region formed between the P-type NiO layer and the N-type Ga_2O_3 channel to achieve effective modulation of the electric field distribution. The heterojunction utilizes the extension of the depletion region at the interface to create a barrier area within the channel, thereby optimizing the internal field profile and enhancing the device's robustness against SEB. Furthermore, the CSG columns, in conjunction with the extended gate field plate, reconfigure the location of the peak electric field away from the conventional gate edge, alleviating local field concentration and improving device reliability under high-voltage and radiation-hard environments.

Results and Discussions Simulation results show that compared to the C-MOSFET, the proposed CSG-MOSFET significantly enhances SEB tolerance. The SEB threshold voltage (V_{SEB}) increases from 240 V to 2 280 V, and the Breakdown Voltage (BV) improves from 2000 V to 3 500 V, while the specific on-resistance is reduced. Consequently, the Baliga figure of merit and the SEB-based figure of merit are dramatically improved. The NiO heterojunction and CSG columns effectively modulate the electric field distribution, relocating the peak field from the gate edge to the gate column edge and alleviating local field concentration, thereby significantly improving radiation hardness.

Conclusions In this paper, a novel radiation-hardened Ga_2O_3 MOSFET design featuring a NiO heterojunction and CSG column structure is proposed through TCAD simulation. The proposed structure significantly enhances SEB tolerance. The V_{SEB} and BV are substantially increased compared to the C-MOSFET, demonstrating superior blocking capability. Due to the charge compensation effect between the P-type NiO layer and the N-type Ga_2O_3 channel, the heterojunction forms an extended depletion region that effectively modulates the electric field distribution within the channel. This modulation alleviates the electric field crowding effect at the conventional gate edge. Furthermore, the CSG columns, in conjunction with the extended gate field plate, actively relocate the peak electric field from the gate edge to the outermost gate column edge. This electric field reconfiguration reduces carrier multiplication effects upon heavy-ion incidence, thereby effectively suppressing SEB. The specific on-resistance is also reduced, leading to improved Baliga figure of merit and SEB-based figure of merit. These advantages make the proposed CSG-MOSFET a promising candidate for power electronics applications in harsh radiation environments such as aerospace and satellite platforms.

Key words: Ga_2O_3 MOSFET; radiation hardening; comb-shaped gate pillar